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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,320	10/29/2003	Franklin Duan	03-1169	7570

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EXAMINER	
NGUYEN, TUNG X	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/696,320	DUAN ET AL.	
	Examiner	Art Unit	
	Tung X. Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 9/30/05.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 December 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,9, 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Lyon et al. (u.s.p 4,972,144).

As to claims 1, 9, Lyon et al. disclose in Figs. 1-4, the method and apparatus for testing a plurality of test structures (111 of figure 2) comprising: a logic circuit to be considered the address lines (112 of figure 2), wherein the logic circuit is configured to receive a triggering signal (TL) from control logic (114 of figure 2); the logic circuit connectable to a plurality of row of the test structures (figure 3A); and the logic circuit configured to sequentially turn on a different single row of the test structures depending on the triggering signal which is received (figure 2, 3A), while other rows remain off, wherein only a single row is active at any given time during the testing and the remaining rows are inactive (col. 5, lines 20-35); and wherein the system is configured to sequentially test the rows of test structures from a first row to a last row, a single row at a time each time the triggering signal changes (col. 5, lines 20-35).

As to claims 16-17, Lyon et al. disclose the logic circuit (112) is resettable wherein none of the test structures (111) are turned on (via 114 of figure 2).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4, 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lyon et al. (u.s.p 4,972,144).

As to claims 2-4, 10-12, Lyon et al. disclose all of limitations except for the logic circuit is connectable to 256 rows of test structures. Lyon et al. disclose in Fig. 2, 3A, the logic circuit couple to the plurality of rows of the test structures for reducing the number of testing, and for reducing cost during testing the plurality of test structures (col. 5, lines 20-35). Thus, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to choose appropriate value of the rows of test structures for reducing the number of tests and reducing cost during testing the plurality of test structures (col. 3, lines 44-47), since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

5. Claims 5-8, 13-15, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lyon et al. (u.s.p 4,972,144), and in view of Kurita et al. (5,289,116).

As to claim 5, Lyon et al. disclose all of the limitations except for the logic circuit comprises an incrementer which is configured to receive the triggering signal. However, Kurita et al. disclose the logic circuit comprises an incrementer to be considered a

counter (TMM of figure 1) for receive the triggering signal and sending signal to test the plurality of test structures (186 of figure 1). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system of Lyon et al., and provides an incrementer, as taught by Kurita et al. for receiving the triggering signal and sending signal to test the plurality of test structures (186 of figure 1).

As to claims 6-7, 13-14, Lyon et al. disclose all of the limitations except for the logic circuit comprises a decoder which is connected to the incrementer. However, Kurita et al. disclose the logic circuit comprises a decoder (ADC/DAC of figure 2) coupled to an incrementer to be a counter (TMM of figure 1) for receiving the triggering signal and sending signal to test the plurality of test structures (186 of figure 1). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system of Lyon et al., and provides a decoder coupled to an incrementer, as taught by Kurita et al. for receiving the triggering signal and sending signal to test the plurality of test structures (186 of figure 1).

As to claims 8, 15, Lyon et al. in view of Kurita et al. disclose all of the limitations except for the incrementer being configured to receive the triggering signal and having eight output lines, and coupled to the decoder. However, Lyon et al., in view of Kurita et al. disclose the logic circuit having the incrementer coupled to the decoder for testing the plurality of rows of the test structures for reducing the number of testing, and for reducing cost during testing the plurality of test structures (col. 5, lines 20-35). Thus, it would have been obvious to one having ordinary skill in the art at the time of the

invention was made to choose appropriate value of the rows of test structures for reducing the number of tests and reducing cost during testing the plurality of test structures (col. 3, lines 44-47), since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

6. Applicant's arguments filed 9/30/05 have been fully considered but they are not persuasive.

In re pages 6-7, to applicant argues Lyon patents does not teach or suggest that only a single row is active at any given time during the testing and the remaining rows are inactive.

In response, the examiner respectfully disagrees with Applicant about the issue for the following the reasons:

Every row of test structures in the test structure array (111 of figure 2) coupled to each address line is examined, only address line A0 is set to a low level and address lines A1-A7 are each set to a high level. If all test structure in row of the test structure array coupled to the address line A0 are normally operating. Thus, it appears (inherently) that the other address lines A1-A7 are each set to a high level coupled to another row of test structures in the test structure array is not examined (col. 5, lines 20-35). Therefore Lyon et al. teach the limitations of wherein only a single row is active at any given time during the testing and the remaining rows are inactive.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung X. Nguyen whose telephone number is (571) 272-1967. The examiner can normally be reached on 8:30am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, ~~Nestor Ramirez~~ Wael Fahmy can be reached on (571) 272-~~2034~~ 1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12/23/05

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TN
12/22/05

12/23/05
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PRIMARY EXAMINER